REMARKS

Claims 1-16 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 112

Applicant traverses the rejection of Claims 1-16 under 35 U.S.C. § 112, second paragraph.

Applicant has provided a substitute FIG. 1 that more accurately depicts the method of the present invention. No new matter is presented by the substitute FIG. 1. Support for the substitute FIG. 1 appears on page 4, lines 2-20 and throughout the detailed description.

The step 12 involves determining a fixed DC level for the DC current bus. This step is self explanatory. In step 14, the DC bus current is regulated to the fixed DC level determined in step 12. In the paragraph beginning on page 5, line 14, one specific implementation for regulating the DC bus current includes positioning a shunt resistor on a negative rail of the voltage source. The voltage drop across the resistor is monitored by the control module. The control module pulse width modulates the transistors based on the voltage drop. Other forms of current regulation may be employed as well.

In step 16, forced current sharing by consecutive phases is performed. Current sharing of the DC bus current occurs by turning off DC bus current to one phase after

turning on DC bus current to a subsequent phase. Page 4, lines 2-20, page 6, lines 8-19, FIGs. 3 and 4.

Applicant respectfully disagrees that the steps set forth in FIG. 1 are not clearly described.

REJECTION UNDER 35 U.S.C. § 102

Applicant traverses the rejection of Claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by Murty (U.S. Pat. No.4,544,868).

Regarding claim 1, Murty does not show teach or suggest a switching circuit that forces current sharing by turning off DC bus current to one phase after turning on DC bus current to a subsequent phase as required by independent apparatus claim 1. Regarding claim 12, Murty does not show teach or suggest the step of a forcing current sharing by turning off DC bus current to one phase after turning on DC bus current to a subsequent phase as required by independent method claim 12.

The forced sharing of the DC bus current creates a sinusoidally-shaped waveform as shown in FIG. 6. Murty does not force sharing of DC bus current and therefore has square wave current waveforms that are similar to the conventional waveforms depicted in FIG. 5 of the present invention (for example, see FIG. 5 of Murty). The BLDC motor of Murty will have acoustic noise problems that are described in the Background of the Invention. Therefore, claims 1 and 12 are allowable. Claims 2-7 and claims 13-16 depend directly or indirectly from claims 1 and 12 and are allowable for the same reasons.

Regarding claim 9, Murty does not show, teach or suggest a control module for selectively enabling the transistors such that each phase of the motor has a phase turn on point that occurs before a phase turn off point of a preceding phase. Therefore, Murty also does not anticipate claim 9 for the reasons set forth above.

Claims 10 and 11 depend directly or indirectly from claim 9 and are allowable for the same reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1211.

Respectfully submitted,

Dated: 6/12/02

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ATTACHMENT FOR SPECIFICATION AMENDMENTS

The following is a marked up version of each replacement paragraph and/or section of the specification in which underlines indicates insertions and brackets indicate deletions.

Please replace the paragraph that begins on page 4, line 21 with the following paragraph:

Turning now to FIG. 2, one approach to the above method is shown. Specifically, it can be seen that a preferred motor control system 20 has a voltage source 30 and an inverter 40. The voltage source 30 (V_{bus}) provides a DC bus current, that is used by a motor 22 to operate an attached load (not shown). The inverter 40 has a phase switching circuit 42 for regulating the DC bus current to a fixed level. The switching circuit 42 forces consecutive phases of the motor to share the bus current at commutation. Specifically, the preferred switching circuit has a plurality of transistors Q1 through Q6 coupled to the motor 22 and the voltage source 30. A control module [46] 46a, 46b, and 46c (collectively reffered to as 46) is coupled to the transistors and can be implemented by any number of hardware/software techniques currently known in the art. For example, the control module 46 may be a microprocessor programmed to execute the required steps discussed herein.

ATTACHMENT FOR CLAIM AMENDMENTS

The following is a marked up version of each amended claim in which underlines indicates insertions and brackets indicate deletions.

1. (Amended) A control system for a motor, the control system comprising:

a voltage source for providing a DC bus current; and

an inverter having a switching circuit for regulating the DC bus current to a fixed level;

said switching circuit forcing consecutive phases of the motor to share the DC bus current at commutation by turning off said DC bus current to one phase after turning on said DC bus current to a subsequent phase.

12. (Amended) A method for controlling a motor, the method comprising the steps of:

determining a fixed level for a DC bus current;

regulating the DC bus current to the fixed level; and

forcing consecutive phases of the motor to share the DC bus current at commutation by turning off said DC bus current to one phase after turning on said DC bus current to a subsequent phase.